1 Megabyte Sync/Sync Burst, Small Outline DIMM

FEATURES

- 2x64Kx72 Synchronous, Synchronous Burst
- Flow-Through Architecture
- Linear and Sequential Burst Support via MODE pin
- Clock Controlled Registered Bank Enables (E1\, E2\)
- Clock Controlled Registered Address
- Clock Controlled Registered Global Write (GW\)
- Aysnchronous Output Enable (G\)
- · Internally self-timed Write
- Individual Bank Sleep Mode enables (ZZ1, ZZ2)
- Gold Lead Finish
- 3.3V +10% Operation
- Access Speed(s): TKHQV=8.5, 10, 12, 15ns
- Common Data I/O
- High Capacitance (30pf) drive, at rated Access Speed
- Single total array Clock
- Multiple Vcc and Gnd

The EDI2CG27264VxxD2 is a Synchronous/Synchronous Burst SRAM, 72 position DIMM (144 contacts) Module, small outline. The Module contains four (4) Synchronous Burst Ram Devices, packaged in the industry standard JEDEC 14mmx20mm TQFP placed on a Multilayer FR4 Substrate. The module architecture is defined as a Sync/Sync Burst, Flow-Through, with support for either linear or sequential burst. This module provides High Performance, 2-1-1-1 accesses when used in Burst Mode, and used as a Synchronous Only Mode, provides a high performance cost advantage over BiCMOS aysnchronous device architectures.

Synchronous Only operations are performed via strapping ADSC\ Low, and ADSP\ / ADV\ High, which provides for Ultra Fast Accesses in Read Mode while providing for internally self-timed Early Writes.

Synchronous/Synchronous Burst operations are in relation to an externally supplied clock, Registered Address, Registered Global Write, Registered Enables as well as an Asynchronous Output enable. This Module has been defined for Quad Word access in both Read and Write Operations.

PINNAMES	DQ0-DQ63	Input/Output Bus
	DQP0-DQP7	Parity Bits
	A0-A15	Address Bus
	E1 E2\	Synchronous Bank Enables
	Clk	Array Clock
	GW	Synchronous Global write Enable
	G\	Asynchronous Output Enable
	ZZ1, ZZ2	Bank Sleep Mode Enables
	Vcc	3.3V Power Supply
	Vss	Gnd

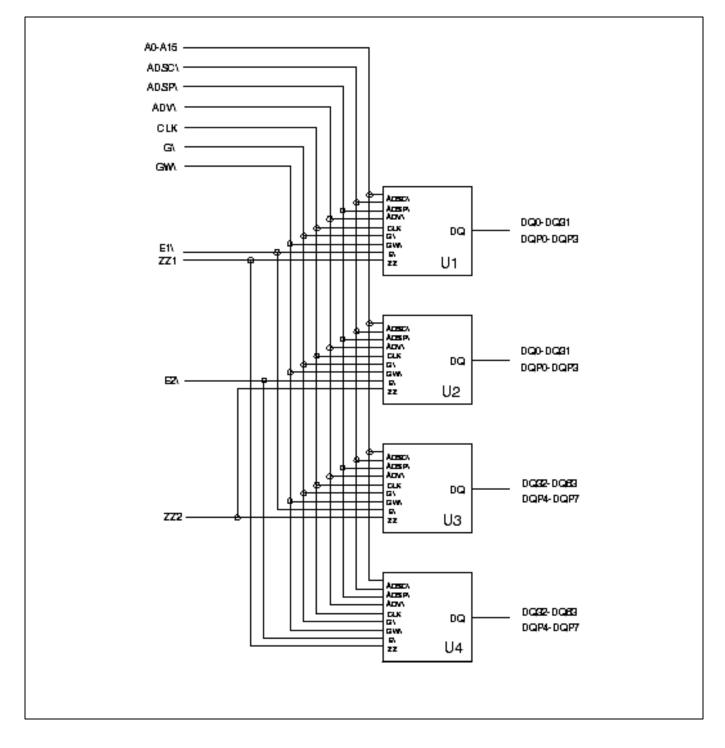


PIN CONFIGURATION

PIN FUNCTION PIN FUNCTION PIN FUNCTION PIN FUNCTION 1 VSS 37 DQ0 73 VSS 109 DQ41 2 VSS 39 DQ7 74 VSS 110 DQ48 3 A0 39 DQ1 75 ZZZ 111 DQ42 4 RRU 40 DQ2 78 DQP3 112 DQ43 6 A1 42 DQ5 77 VCC 113 DQ43 7 A2 43 DQ2 78 VCC 114 DQ44 7 A2 43 DQ2 79 DQ24 115 VSS 8 A14 45 VSS 81 DQ25 117 RRU 10 A3 48 VSS 82 DQ30 118 VCC 12 A13 48 DQ91 84 DQ29 120 VCC <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th> <th></th>								
1 10 </td <td>PIN</td> <td>FUNCTION</td> <td>PIN</td> <td>FUNCTION</td> <td>PIN</td> <td>FUNCTION</td> <td>PIN</td> <td>FUNCTION</td>	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
3 A0 39 DQ1 75 ZZ2 111 DQ42 4 RRJ 40 DQ8 78 DQP3 112 DQ43 5 RRJ 41 DQ2 78 DQP3 112 DQ43 6 A1 42 DQ5 77 VCC 113 DQ44 7 A2 43 DQ3 79 DQ24 115 VSS 8 A15 44 DQ4 80 DQ31 118 VSS 9 A14 45 VSS 81 DQ25 117 RRJ 10 A3 48 VSS 82 DQ30 118 DQ98 11 A4 47 ZZ1 83 DQ24 110 VCC 12 A13 48 DQ91 84 DQ29 120 VCC 13 A12 49 VCC 85 DQ27 121 DQ48	1	VSS	37	DQ0	73	VSS	109	DQ41
4 RRJ 40 DQ8 78 DQP3 112 DQ45 5 RRJ 41 DQ2 77 VCC 113 DQ43 8 A1 42 DQ5 77 VCC 114 DQ44 7 A2 43 DQ3 78 VCC 114 DQ44 7 A2 43 DQ4 90 DQ31 118 VSS 8 A15 44 DQ4 90 DQ31 118 VSS 9 A14 45 VSS 81 DQ25 117 RIJ 10 A3 48 VSS 82 DQ30 118 DQP8 11 A4 47 ZZ1 83 DQ29 120 VCC 13 A12 49 VCC 85 DQ27 121 DQ48 14 A5 50 VCC 86 DQ29 122 DQ56 <	2	VSS	38	DQ7	74	VSS	110	DQ48
5 RRJ 41 DG2 77 VCC 113 DQ43 8 A1 42 DG5 78 VCC 114 DG44 7 A2 43 DG2 78 VCC 114 DG44 7 A2 43 DG2 79 DG24 115 VSS 8 A15 44 DG4 80 DG21 118 VSS 9 A14 45 VSS 81 DG25 117 RRJ 10 A3 48 VSS 82 DG20 118 DG26 11 A4 47 ZZ1 83 DG28 119 VCC 12 A13 48 DGP1 84 DG29 120 VCC 13 A12 49 VCC 85 DG27 121 DG48 14 A5 50 VCC 86 DG29 122 DG55	Э	AO	39	DQ1	75	ZZ2	111	DQ42
B A1 42 DQ5 78 VCC 114 DQ44 7 A2 43 DQ3 79 DQ24 115 VSS 8 A15 44 DQ4 90 DQ31 118 VSS 9 A14 45 VSS 81 DQ25 117 RRJ 10 A3 48 VSS 81 DQ25 117 RRJ 10 A3 48 VSS 82 DQ30 118 DQP8 11 A4 47 ZZ1 83 DQ24 102 VCC 12 A13 48 DQP1 84 DQ29 120 VCC 13 A12 49 VCC 85 DQ29 122 DQ48 14 A5 50 VCC 86 DQ29 122 DQ49 18 A11 52 DQ15 89 RRJ 125 DQ50	4	RRJ	40	DQ8	78	DQP3	112	DQ45
7 A2 43 DCg3 79 DCg24 115 VSS 8 A15 44 DCq4 80 DCg31 116 VSS 9 A14 45 VSS 81 DCg25 117 RRJ 10 A3 48 VSS 82 DCg30 118 DCg78 11 A4 47 ZZ11 82 DCg28 119 VCC 12 A13 48 DCg71 84 DCg29 120 VCC 13 A12 49 VCC 85 DCg29 122 DCg55 15 A8 51 DCg8 87 VSS 123 DCq49 18 A11 52 DCq15 89 RRJ 125 DCq50 19 A7 54 DCq14 90 DCqP4 128 DCq51	5	RRJ	41	002	Π	VCC	113	DQ43
B A15 44 DC44 B0 DC231 118 VSS 9 A14 45 VSS B1 DC25 117 RRJ 10 A3 48 VSS B2 DC20 118 DC48 11 A4 47 ZZ1 B2 DC28 117 RRJ 12 A13 48 DC491 B4 DC28 120 VCC 13 A12 49 VCC B5 DC29 120 VCC 14 A5 50 VCC B6 DC29 122 DC48 18 A11 52 DC15 B9 VSS 123 DC49 18 A7 54 DC14 90 DC194 128 DC35	8	A1	42	DQ5	78	VCC	114	DQ44
9 A14 45 VSS B1 DG25 117 RRJ 10 A3 48 VSS B2 DG20 118 DGP8 11 A4 47 ZZ1 B2 DG28 119 V0C 12 A13 48 DGP1 B4 DG29 120 VCC 13 A12 49 VCC B5 DG29 122 DG48 14 A5 50 VCC B6 DG29 122 DG48 18 A11 52 DG15 B7 VSS 123 DG49 18 A11 52 DG16 B9 RRJ 125 DG50 19 A7 54 DG14 90 DGP4 128 DG35	7	A2	43	003	79	DC424	115	VSS
10 A3 48 VSS B2 DQ30 118 DQP8 11 A4 47 ZZ1 B3 DQ28 119 VCC 12 A13 48 DQP1 B4 DQ29 120 VCC 13 A12 49 VCC B5 DQ29 122 DQ48 14 A5 50 VCC B5 DQ29 122 DQ48 18 A11 52 DQ15 B7 VSS 123 DQ49 18 A11 52 DQ15 B9 RRJ 125 DQ50 19 A7 54 DQ14 90 DQP4 128 DQ53	8	A15	44	004	80	DCG91	118	VSS
11 A4 47 ZZ1 B3 DG28 119 V00 12 A13 48 DGP1 B4 DG29 120 V00 13 A12 49 V00 B5 DG29 120 V00 14 A5 50 V00 B5 DG29 122 DG48 14 A5 50 V00 B5 DG29 122 DG49 18 A11 52 DG15 B9 VSS 123 DG49 17 A10 53 DG9 B9 RB1 125 DG50 18 A7 54 DG14 90 DGP4 128 DG53	9	A14	45	VSS	81	DC25	117	RRJ
12 A13 48 DQP1 B4 DQ23 120 VCC 13 A12 49 VCC B5 DQ27 121 DQ48 14 A5 50 VCC B6 DQ28 122 DQ45 15 A8 51 DQ9 B7 VSS 123 DQ49 18 A11 52 DQ15 B9 VSS 124 DQ54 17 A10 53 DQ9 B9 RRJ 125 DQ50 18 A7 54 DQ14 90 DQP4 128 DQ53	10	A3	48	VSS	82	DC 3 0	118	DQP8
13 A12 49 VCC B5 DG27 121 DG48 14 A5 50 VCC B6 DG29 122 DG55 15 A8 51 DG9 B7 VSS 123 DG49 18 A11 52 DG15 B9 VSS 123 DG49 17 A10 53 DG9 B9 RRJ 125 DG50 18 A7 54 DG14 90 DGP4 128 DG53	11	A4	47	ZZ1	89	DC28	119	VCC
14 A5 50 VCC B8 DCQ29 122 DCQ55 15 A8 51 DCQ9 B7 VSS 123 DCQ49 18 A11 52 DC15 B9 VSS 124 DC354 17 A10 53 DC49 B9 RRJ 125 DC450 18 A7 54 DC14 90 DC194 128 DC350	12	A13	48	DQP1	B4	DC(29	120	VCC
15 A8 51 DQ8 B7 VSS 123 DQ49 18 A11 52 DQ15 B8 VSS 124 DQ54 17 A10 53 DQ9 B9 RRJ 125 DQ50 18 A7 54 DQ14 90 DQP4 128 DQ53	13	A12	49	VCC	85	DC#27	121	DC448
18 A11 52 DQ15 BB VSS 124 DQ54 17 A10 53 DQ9 B9 RRJ 125 DQ50 18 A7 54 DQ14 90 DQP4 128 DQ53	14	A5	50	VCC	88	DC29	122	DQ55
17 A10 53 DQ9 B9 RRJ 125 DQ50 18 A7 54 DQ14 90 DQP4 128 DQ53	15	AB	51	DQB	87	VSS	123	DC49
18 A7 54 DQ14 90 DQP4 128 DQ53	18	A11	52	DQ15	88	VSS	124	DQ54
	17	A10	53	DQ9	89	RRJ	125	0Q50
19 Ag 55 DQ10 91 VCC 127 DQ51	18	A7	54	DQ14	90	DQP4	128	DQ53
	19	AB	55	DQ10	91	VCC	127	DQ51
20 A9 56 DQ13 S2 VCC 128 DQ52	20	A9	58	DQ13	92	VCC	129	0Q52
21 VCC 57 DQ11 59 DQ22 129 VSS	21	VCC	57	DQ11	89	0032	129	VSS
22 VCC 58 DQ12 94 DQ29 130 VSS	22	VCC	58	DQ12	94	0039	130	VSS
23 GA 59 VSS 95 DQ23 131 RRJ	23	G	59	VSS	95	0033	191	RRJ
24 RRJ 60 VSS 98 DQ99 132 DQ97	24	RRJ	60	VSS	98	DCGE	132	DQP7
25 GWA 81 E2A 97 DQ84 133 VCC	25	GWA	81	EZ\	97	DC434	133	VCC
28 ADV. 82 DQP2 98 DQ97 134 VOC	28	ADV.	62	DQP2	98	DC(37	134	VCC
27 ADSPA 83 VCC 39 DQ35 135 DQ58	27	ADSP\	63	VCC	39	DC35	135	DQ58
28 ADSC\ 64 VCC 100 DQ28 138 DQ83	28	ADSC\	64	VCC	100	DCC38	138	00,69
29 MODE 65 DQ16 101 VSS 137 DQ57	29	MODE	65	DQ18	101	VSS	137	DQ57
30 CLK 88 DQ23 102 VSS 138 DQ82	30	CLK	88	DC23	102	VSS	199	00,62
31 VSS 67 DQ17 103 RRJ 139 DQ69	91	VSS	67	DQ17	103	RRJ	139	DQ59
32 VSS 69 DQ22 104 DQP5 140 DQ81	32	VSS	68	DQ22	104	DQP5	140	DQ81
33 E1\ 69 DQ18 105 VCC 141 DQ59	33	E1\	69	DQ18	105	VCC	141	DQ59
34 DQP0 70 DQ21 108 VCC 142 DQ80	34	DQP0	70	DC21	108	VCC	- 142	DC,80
35 V0C 71 DQ19 107 DQ40 143 VSS	35	VCC	71	DQ19	107	DC40	143	VSS
38 VCC 72 DQ20 108 DQ47 144 VSS	36	VCC	72	DC#20	108	DQ47	144	VSS

WHITE ELECTRONIC DESIGNS

FUNCTIONAL BLOCK DIAGRAM



WHITE ELECTRONIC DESIGNS

PIN DESCRIPTIONS

DIMM Pins	Symbol	Туре	Description
3, 6, 7, 10, 11, 14		Input	Addresses: These inputs are registered and must meet the setup and hold
15, 18, 19, 20, 17		Synchronous	times around the rising edge of CLK. The burst counter generates internal
16, 13, 12, 9, 8, 3			addresses associated with A0 and A1, during burst and wait cycle.
25	GW	Input	Global Write: This active LOW input allows a full 72-bit WRITE to occur
		Synchronous	independent of the BWE\ and BWx\ lines and must meet the setup and hold
			times around the rising edge of CLK.
30	CLK	Input	Clock: This signal registers the addresses, data, chip enables, write control
		Synchronous	and burst control inputs on its rising edge. All synchronous inputs must
			meet setup and hold times around the clock's rising edge.
33,61	E1 E2\	Input	Bank Enables: These active LOW inputs are used to enable each
		Synchronous	individual bank and to gate ADSP\.
23	G\	Input	Output Enable: This active LOW asynchronous input enables the data output
			drivers.
26	ADV	Input	Address Status Processor: This active LOW input is used to control the
		Synchronous	internal burst counter. A HIGH on this pin generates wait cycle (no address
		5	advance).
27	ADSP\	Input	Address Status Processor: This active LOW input, along with EL\ and EH\
	Synchronous	•	being LOW, causes a new external address to be registered and a READ
	5		cycle is initiated using the new address.
28	ADSC\	Input	Address Status Controller: This active LOW input causes device to be de-
	Synchronous	·	selected or selected along with new external address to be registered. A
	J		READ or WRITE cycle is initiated depending upon write control inputs.
29	MODE	Input Static	Mode: This input selects the burst sequence. A LOW on this pin selects
		·	LINEAR BURST. A NC or HIGH on this pin selects INTERLEAVED
			BURST.
47,75	ZZ1, ZZ2,	Input	Snooze: These active HIGH inputs put the individual banks in low powe
		Asynchronous	consumption standby mode. For normal operation, this input
			has to be either LOW or NC (no connect).
Various	DQ0-63	Input/Output	Data Inputs/Outputs: First byte is DQ0-7, second byte is DQ8-15, third byte is
			DQ16-23, fourth byte is DQ24-31, fifth byte is DQ32-39, sixth byte is
			DQ40-47, seventh byte is DQ48-55 and the eight byte is DQ56-64.
34, 48, 62, 76,	DQP0-7	Input/Output	Parity Inputs/Outputs: DQP0 is parity bit for DQ0-7. DQP1 is parity bit for
			DQ8-15.
90, 104, 118,132			DQP2 is parity bit for DQ16-23. DQP3 is parity bit for DQ24-31. DQP4 is
			parity bit for DQ32-39. DQP5 is parity bit for DQ40-47. DQP6\ is parity bit for
			DQ48-55. DQP7 is parity bit for DQ56-64 and DQP7. In order to use the devi
			configured as a 128K x 64, the parity bits need to be tied to Vss through a 10k
			5 · · · · · · · · · · · · · · · · · · ·
dlan			
	Witte	E ELEC	CTRONIC DESIGNS
	VVH	F FIFE	TRONIC DESIGNS ohm resistor.

Various	Vcc	Supply	Core power supply: +3.3V -5%/+10%
Various	Vss	Ground	Ground



SYNCHRONOUS BURST - TRUTH TABLE

Operation	E1\	E2\		ADSC\				CLK	DQ	Addr. Used
Deselected Cycle, Power Down; Bank	1 H	Х	Х	L	Х	Х	Х	L-H	High-Z	None
Deselected Cycle, Power Down; Bank	2 X	Η	Х	L	Х	Х	Х	L-H	High-Z	None
Read Cycle, Begin Burst; Bank 1	L	Η	L	Х	Х	Х	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	Н	L	Х	Х	Х	Н	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	Η	L	L	Х	Х	Х	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	Н	L	L	Х	Х	Х	Н	L-H	High-Z	External
Write Cycle, Begin Burst; Bank 1	L	Η	Н	L	Х	L	Х	L-H	D	External
Write Cycle, Begin Burst; Bank 2	Η	L	Н	L	Х	L	Х	L-H	D	External
Read Cycle, Begin Burst; Bank 1	L	Η	Н	L	Х	Н	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 1	L	Η	Н	L	Х	Н	Η	L-H	High-Z	External
Read Cycle, Begin Burst; Bank 2	Η	L	Н	L	Х	Н	L	L-H	Q	External
Read Cycle, Begin Burst; Bank 2	Н	L	Н	L	Х	Н	Н	L-H	High-Z	External
Read Cycle, Continue Burst; Bank 1	Х	Н	Х	H	L	Н	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	Х	Н	Х	H	L	Н	Н	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	Н	Х	Х	H	L	Н	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	Н	Х	Х	H	L	Н	Н	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 1	Н	Н	Х	H	L	Н	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 1	Н	Η	Х	Н	L	Н	Н	L-H	High-Z	Next
Read Cycle, Continue Burst; Bank 2	Н	Η	Х	Н	L	Н	L	L-H	Q	Next
Read Cycle, Continue Burst; Bank 2	Н	Н	Х	Н	L	Н	Н	L-H	High-Z	Next
Write Cycle, Continue Burst; Bank 1	Х	Н	Н	Н	L	L	Х	L-H	D	Next
Write Cycle, Continue Burst; Bank 1	Н	Н	Х	Н	L	L	Х	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	Н	Х	Н	Н	L	L	Х	L-H	D	Next
Write Cycle, Continue Burst; Bank 2	Н	Н	Х	Н	L	L	Х	L-H	D	Next
Read Cycle, Suspend Burst; Bank 1	Х	Н	Н	H	Н	Н	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	Х	Н	Н	Н	Н	Н	Н	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	Н	Х	Н	Н	Н	Н	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	Н	Х	Н	Н	Н	Н	Н	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 1	Н	Н	Х	Н	Н	Н	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 1	Н	Н	Х	Н	Н	Н	Н	L-H	High-Z	Current
Read Cycle, Suspend Burst; Bank 2	Н	Н	Х	Н	Н	Н	L	L-H	Q	Current
Read Cycle, Suspend Burst; Bank 2	Н	Н	Х	Н	Н	Н	Н	L-H	High-Z	Current
Write Cycle, Suspend Burst; Bank 1	Х	Н	Н	Н	Н	L	Х	L-H	D	Current
Write Cycle, Suspend Burst; Bank 1	H	H	X	H	H	L	Х	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	Н	Х	Н	H	H	L	Х	L-H	D	Current
Write Cycle, Suspend Burst; Bank 2	H	Н	X	H	H		Х	L-H	D	Current



WHITE ELECTRONIC DESIGNS

SYNCHRONOUS ONLY - TRUTH TABLE

Operation	E1\	E2\	GW\	G\	ZZ	CLK	DQ
Synchronous Write-Bank 1	L	Н	L	Н	L	٨	High-Z
Synchronous Read-Bank 1	L	Н	Н	L	L	٨	-
Synchronous Write-Bank 2	Н	L	L	Н	L	٨	High-Z
Synchronous Read-Bank 2	Н	L	Н	L	L	٨	
Synchronous Write-Bank 3	Н	Н	L	Н	L	4	High-Z
Synchronous Read-Bank 3	Н	Н	Н	L	L	•	
Synchronous Write-Bank 4	Н	Н	L	Н	L	*	High-Z
Synchronous Read-Bank 4	Н	Н	Н	L	L	•	
Snooze Mode	Х	Х	Х	Х	Н	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
Vin	-0.5V to Vcc +0.5V
Storage Temperature	-55°C to +125°C
Operating Temperature (Commercial) 0°C to +70°C
Operating Temperature (Industrial)	-40°C to +85°C
Short Circuit Output Current	10 mA

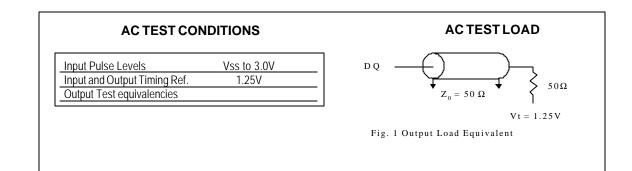
"Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Тур	Мах	Units
Supply Voltage	VCC	3.14	3.3	3.6	V
Supply Voltage	VSS	0.0	0.0	0.0	V
InputHigh	ΜH	1.1	3.0	VCC+0.3	V
InputLow	VIL	-0.3	0.0	0.3	V
Input Leakage	ILi	-2	1	2	μA
Output Leakage	ILo	-2	1	2	μA

DC ELECTRICAL CHARACTERISTICS - READ CYCLE

					N	lax
SYM	Тур	8.5	9	10	12	Units
lcc1	1.55	2.2	2.1	2.1	2.0	А
lcc	750	1.5	1.5	1.0	1.0	Α
IccZZ	150	220	210	200	200	mA
Icc3	400	700	700	625	600	mA
IccK	600	1.0	1.0	.75	.75	Α
	Icc1 Icc IccZZ Icc3	Icc1 1.55 Icc 750 IccZZ 150 Icc3 400	lcc1 1.55 2.2 lcc 750 1.5 lccZZ 150 220 lcc3 400 700	lcc1 1.55 2.2 2.1 lcc 750 1.5 1.5 lccZZ 150 220 210 lcc3 400 700 700	Icc1 1.55 2.2 2.1 2.1 Icc 750 1.5 1.5 1.0 IccZZ 150 220 210 200 Icc3 400 700 700 625	SYM Typ 8.5 9 10 12 lcc1 1.55 2.2 2.1 2.1 2.0 lcc 750 1.5 1.5 1.0 1.0 lccZ 750 20 210 200 200 lccZZ 150 220 210 200 200 lcc3 400 700 700 625 600





BURST ADDRESS TABLE (MODE=NC/VCC)

BURST ADDRESS TABLE (MODE=GND)

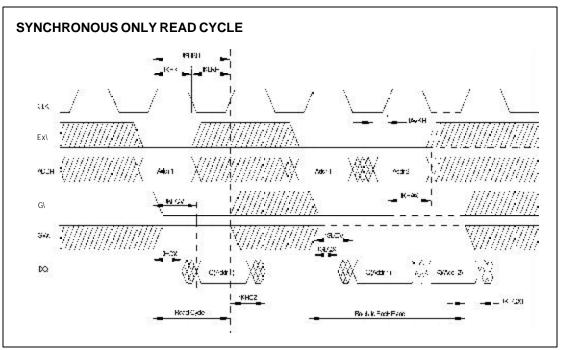
First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
AA00	AA01	AA10	AA11
AA01	AA00	AA11	AA10
AA10	AA11	AA00	AA01
AA11	AA10	AA01	AA00

First Address (external)	Second Address (internal)	Third Address (internal)	Fourth Address (internal)
AA00	AA01	AA10	AA11
AA01	AA10	AA11	AA00
AA10	AA11	AA00	AA01
AA11	AA00	AA01	AA10

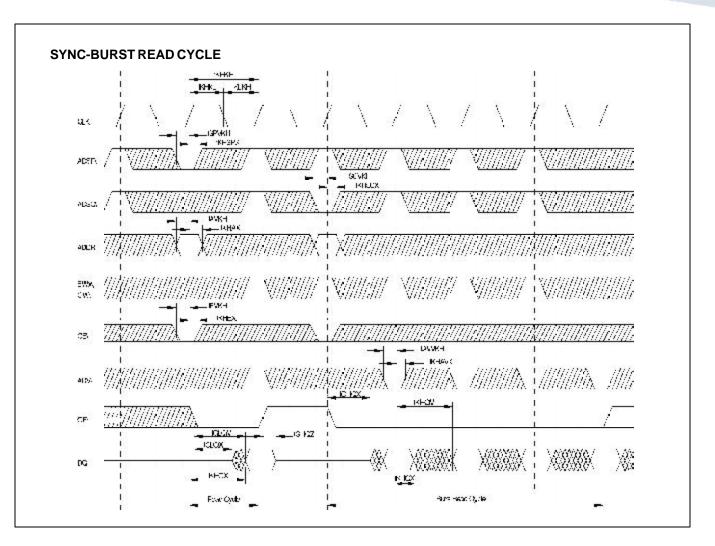
READ CYCLE TIMING PARAMETERS

		8.5	ins	9	ns	10	ns	12	ns	
Description	Sym	Min	Мах	Min	Мах	Min	Max	Min	Мах	Units
Clock Cycle Time	tKhKh	*	*	10		12		15		ns
Clock High Time	tKHKL	*	*	5		5		5		ns
Clock Low Time	tKLKH	*	*	5		5		5		ns
Clock to Output Valid	tKHQV	*	*		9		10		12	ns
Clock to Output Invalid	tKHQX1	*	*	3		3		3		ns
Clock to Output Low-Z	tKHQX	*	*	2		2		2		ns
Output Enable to Output Valid	tGLQV	*	*		4		4		5	ns
Output Enable to Output Low-Z	tGLQX	*	*	0		0		0		ns
Output Enable to Output High-Z	tGHQZ	*	*		4		4		5	ns
Address Setup	tAVKH	*	*	2.5		2.5		2.5		ns
Bank Enable Setup	tEVKH	*	*	2.5		2.5		2.5		ns
Address Hold	tKHAX	*	*	1.0		1.0		1.0		ns
Bank Enable Hold	tKHEX	*	*	1.0		1.0		1.0		ns

*TBD



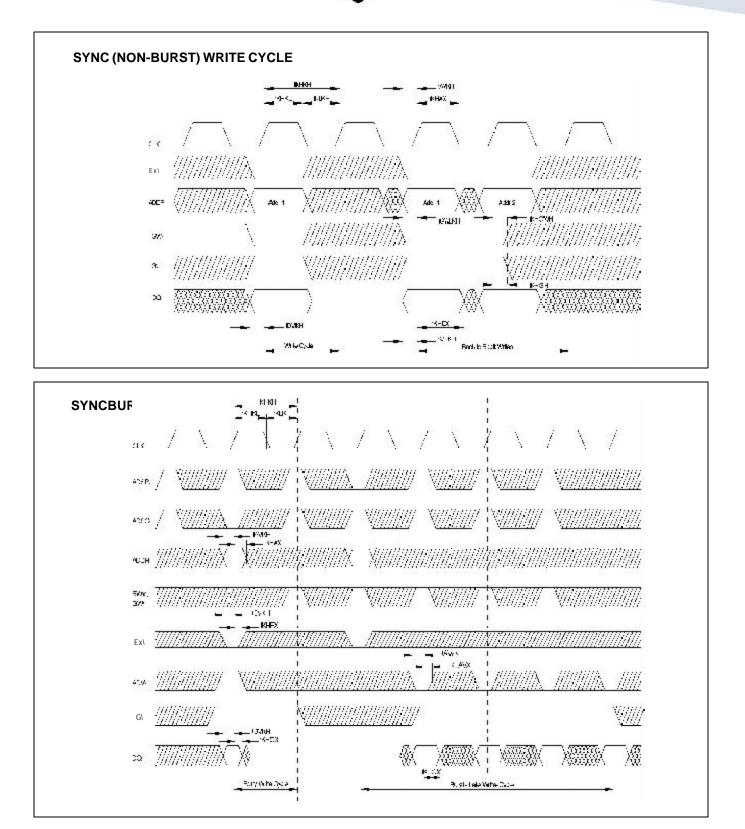
WHITE ELECTRONIC DESIGNS



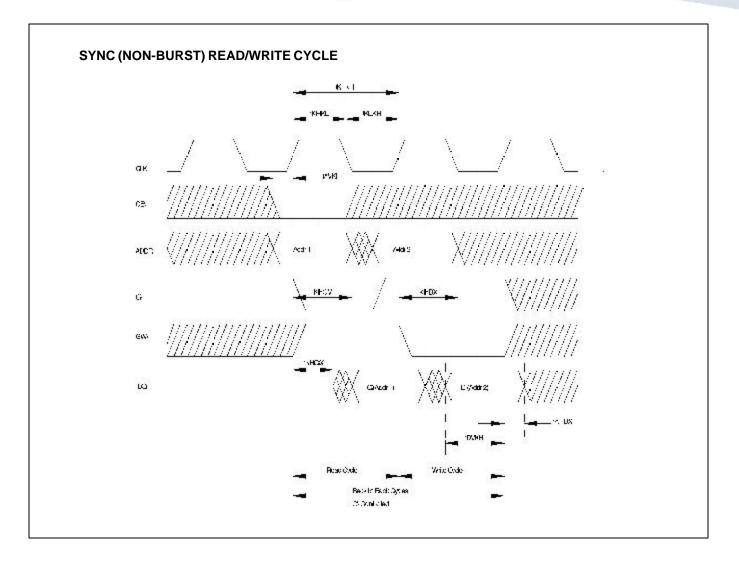
WRITE CYCLE TIMING PARAMETERS

		8.5	ōns	91	าร	10	ns	12	ns	
Description	Sym	Min	Мах	Min	Max	Min	Мах	Min	Мах	Units
Clock Cycle Time	tKHKH			10		12		15		ns
Clock High Time	tKHKL			4		4		5		ns
Clock Low Time	tKLKH			4		4		5		ns
Address Setup	tAVKH			2.5		2.5		2.5		ns
Address Hold	tKHAX			1.0		1.0		1.0		ns
Bank Enable Setup	tEVKH			2.5		2.5		2.5		ns
Bank Enable Hold	tKHEX			1.0		1.0		1.0		ns
Global Write Enable Setup	tWVKH			2.5		2.5		2.5		ns
Global Write Enable Hold	tKHWX			1.0		1.0		1.0		ns
Data Setup	tDVKH			2.5		2.5		2.5		ns
DataHold	tKHDX			1.0		1.0		1.0		ns

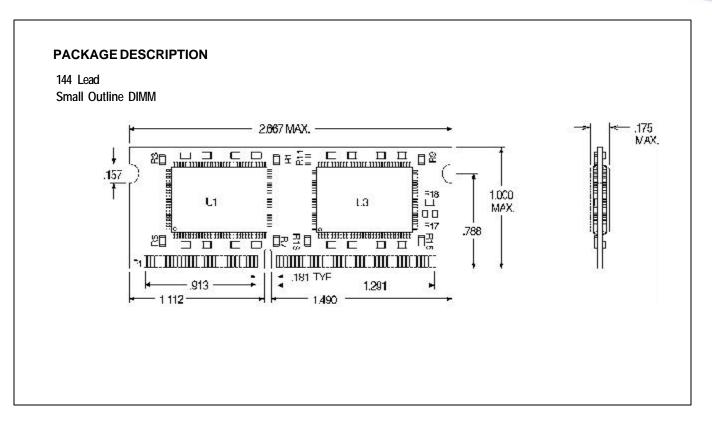
WHITE ELECTRONIC DESIGNS











PartNumber	Organization	Voltage	Speed (ns)	Package
DI2CG27264V85D1*	2x64Kx72	3.3	8.5	144 Small Outline DIMM
DI2CG27264V9D1*	2x64Kx72	3.3	9	144 Small Outline DIMM
DI2CG27264V10D1	2x64Kx72	3.3	10	144 Small Outline DIMM
DI2CG27264V12D1	2x64Kx72	3.3	12	144 Small Outline DIMM